REMARKS:

Claims 23-31 are pending in the present application. Claims 23-31 were rejected in the Office Action dated July 12, 2004. Reconsideration of all pending claims is requested in light of the arguments presented below.

Claim 24 was rejected under 35 USC 103(a) as being unpatentable over Iwasa (US Patent 5,471423) in view of Shin (US Patent 6,180,457). Claim 24 recites, "electrically conductive control gates... protruding downward into slots formed in the field dielectric between adjacent ones of the charge storage elements." The Office Action stated, "Iwasa lacks slots formed in the field dielectric." The Office Action cited Shin (Fig. 17 and column 8, lines 10-32) as teaching this claim element. The motivation provided to combine these references was "for self-alignment." It is submitted that Shin does not show the slots of claim 24 and that no adequate motivation is provided for combining the two cited references.

Claim 24 recites, "slots formed in the field dielectric between adjacent ones of the charge storage elements." In contrast, Shin appears to show reduced thickness of isolation layer 20 at a different location. Specifically, Shin appears to show that isolation layer 20 is thinner at an intermediate location between rows of charge storage elements. Figures 16 and 17 of Shin show two cross-sections of a memory array. These two cross sections are taken along X1-X1' and X2-X2' respectively, as shown in Figure 3. Figure 16 shows a portion of isolation layer 210 that appears to have its original thickness. This portion of isolation layer 210 has floating gates 330 on either side. There does not appear to be any slot formed in this portion of isolation layer 210. Figure 17 shows a portion of isolation layer 210 that has a reduced thickness. However, this portion of isolation layer 210 does not appear to be "between adjacent ones of the charge storage elements." Thus, the reduced thickness in this area does not appear to be a "slot formed in the field dielectric between adjacent ones of the charge storage elements" of claim 24. Because this claim element has not been shown, it is submitted that a prima facie case of obviousness has not been made with respect to claim 24.

The Office Action stated, "it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Shin into the Iwasa reference for self-alignment."

However, it is not understood how combining these teachings would improve self-alignment. Both Shin and Iwasa appear to disclose self-aligned processes. Shin discloses "a floating gate 330 and an interlayer insulating layer pattern 410 to be self-aligned with the control gate 610 are formed as shown in FIGS. 16 and 18." Column 7, lines 58-60. Iwasa discloses "The polycrystalline silicon layer 25, second gate insulating film 24, polycrystalline silicon layer 23, and first gate insulating film 22 are sequentially self-etched in that order by the reactive ion etching method. The photoresist 32 is removed after that, thereby forming the floating gate, control gate of each memory cell and the shield gate." Column 10, lines 18-23. It is not understood how self-alignment could provide a motivation to combine references each of which appears to teach self-alignment.

In addition, Shin appears to teach away from the cited combination. The particular feature of Shin that is cited in the Office Action (reduced thickness of isolation layer 210) appears to be a negative aspect of the process disclosed. Shin discloses with respect to a similar structure in Figure 1, "This undesired etching of the isolation layer 20 becomes excessive with the high integration of a non-volatile memory device, and hence, may cause several problems." Column 1, lines 62-64. Shin further details the problem with respect to Figures 1 and 17 in column 9, lines 1-26. For example, "the isolation layer 210 of FIG 17 can be reduced to a thickness of 100A, so that the process margin of ion implantation is reduced." Column 9, lines 1-3. Thus, the reduced thickness of isolation layer 210 of Shin appears to be an unwelcome effect of the process disclosed. Rather than suggesting the combination of this feature with the teaching of Iwasa, Shin appears to teach away from such a combination because he describes this feature as generating defects. "The generation of such a defect degrades the isolation characteristics." Column 9, lines 22-23. Thus, no adequate motivation to combine the references appears to have been provided and the references appear to teach away from such a combination.

In summary, the cited prior art does not appear to show all the limitations of claim 24 and specifically does not appear to show "slots formed in the field dielectric between adjacent ones of the charge storage elements." The motivation cited for combining these references is not understood and one of the references appears to teach away from such a

combination. Therefore, it is submitted that a prima facie case of obviousness has not been made and it is requested that the rejection be withdrawn.

Claims 25-27 depend from claim 24 and are therefore submitted to be allowable at least for depending from an allowable base claim. In addition, claims 25-27 include features that have not been identified in the cited references. For example, claim 25 recites limitations with regard to top and bottom portions of a charge storage element, but these portions have not been identified in the cited references. Claim 27 recites a particular structure having "select gates and source/drain regions in the substrate alternately positioned between adjacent storage elements along the rows." This limitation has not been identified in the cited references. Therefore, claims 25-27 are submitted to be additionally allowable over the cited references as containing claim elements that were not identified in the cited references.

Claim 28 was rejected for the same reasons given with respect to claim 24. Claim 28 is amended to have the limitation "the control gates additionally extending between adjacent charge storage elements for a distance greater than a thickness of the second portion of the charge storage elements." This limitation is not believed to be shown by the cited references. The Office Action did not identify the first and second portions of a charge storage unit in either cited reference. However, both references appear to show a control gate that extends between charge storage elements to an extent that is less than the thickness of the portion of the charge storage unit that is adjacent to the protruding portion of the control gate (see Figure 7 of Iwasa and Figure 16 of Shin). Because the first and second portions of claim 28 were not identified in the references, it is submitted that a prima facie case of obviousness has not been made with respect to claim 28. In addition, if such portions were identified it is not seen how they would provide the basis for a rejection because of the limitation above regarding the control gate. Therefore, it is submitted that claim 28 is allowable over the cited references.

Claims 29-31 are submitted to be allowable at least for depending from an allowable base claim. In addition, claims 29-31 recite additional elements that have not been identified in the cited references. For example, claim 31 recites, "two charge storage elements between adjacent substrate source and drain regions and a select transistor between the two charge storage elements." This limitation has not been identified in the

cited references and does not appear to be shown. Therefore, claim 31 is submitted to be additionally allowable over the cited references.

New claims 32-36 are added by this amendment. New claims 32-36 are supported throughout the specification and are believed to be allowable for similar reasons to those given with respect to claims 24 and 28. In particular, independent claim 32 includes the limitations "protrusions of the elongated conductive element extending between adjacent charge storage elements to a level that is closer to the substrate surface than the plane is to the substrate surface." This limitation does not appear to be shown by the cited references.

Accordingly, it is believed that all pending claims are now in condition for allowance and an indication of their allowance is respectfully requested. However, if the Examiner is aware of any issues that should be addressed, a phone call to the undersigned at: (415) 318-1160 would be appreciated.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 12, 2004.

Franklin Dyer

Respectfully submitted,

Gerald P. Parsons 10/12/04
Gerald P. Parsons Date
Reg. No. 24,486